What Is Claimed Is:

1. A method for performing a computation generally expressible in the form $d = \sum_{i=0}^{N-1} a(i) * b(i)$ comprising:

   (a) determining a common factor 'c' such that

   $$d = c\left(\sum_{i=0}^{N-1} a(i) * b'(i)\right)$$ wherein at least one of the b'(i)'s is unity;

   (b) utilizing at least one MAAC kernel to carry out the computation, wherein the at least one MAAC kernel is utilized as a function of a coefficient b'(i) being unity.

2. The method according to claim 1, wherein the MAAC kernel includes a multiplier block, an adder block and a register block, wherein an output of the multiplier block is coupled to an input of the adder block, an output of the adder block is coupled to an input of the register block and an output of the register block is coupled to a second input of the adder block and the adder block receives at its second input an additional addend.

3. The method according to claim 2, wherein the terms a(i) are input data terms and the terms b(i) and b'(i) are coefficients.

4. The method according to claim 3, wherein (c) further includes if a coefficient b'(i) is unity, utilizing a MAAC kernel such that the additional addend is an input term that would be multiplied by the unity coefficient b'(i).

5. The method according to claim 4, wherein the numerical computation is an IDCT computation.

6. The method according to claim 5, wherein an eight-point IDCT is computed utilizing the following expression:

$$\begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \end{bmatrix} = \frac{1}{2} A' \begin{bmatrix} y_0 \\ y_4 \\ y_2 \\ y_6 \end{bmatrix} + \frac{1}{2} B' \begin{bmatrix} y_1 \\ y_5 \\ y_3 \\ y_7 \end{bmatrix} \quad \begin{bmatrix} x_7 \\ x_6 \\ x_5 \\ x_4 \end{bmatrix} = \frac{1}{2} A' \begin{bmatrix} y_0 \\ y_4 \\ y_2 \\ y_6 \end{bmatrix} - \frac{1}{2} B' \begin{bmatrix} y_1 \\ y_5 \\ y_3 \\ y_7 \end{bmatrix}$$

where:

$$A' = \begin{bmatrix} 1 & 1 & c'(2) & c'(6) \\ 1 & -1 & c'(6) & -c'(2) \\ 1 & -1 & -c'(6) & c'(2) \\ 1 & 1 & -c'(2) & -c'(6) \end{bmatrix} \quad B = \begin{bmatrix} c'(1) & c'(5) & c'(3) & c'(7) \\ c'(3) & -c'(1) & -c'(7) & -c'(5) \\ c'(5) & c'(7) & -c'(1) & c'(3) \\ c'(7) & c'(3) & -c'(5) & -c'(1) \end{bmatrix}$$

7. A computational kernel for carrying out numerical computations including:

a multiplier block;

an adder block;

a register block;

wherein an output of the multiplier block is coupled to a first input of the adder block, an output of the adder block is coupled to an input of the register block and an output of the register block is coupled to a second input of the adder block, the adder block receiving a third input.

8. The computational kernel according to claim 7, wherein the additional input provided to the adder block is an input datum associated with a unity coefficient and the multiplier block receives an input coefficient.

9. A computational architecture kernel for carrying out numerical computations including:

a multiplier block;

a first adder block;

a second adder block

a register block;

wherein the first adder block receives two inputs (e(i) and a(i)) and an output of the first adder block is coupled to a first input of the multiplier block, the multiplier block receiving a second input (b(i)) and an output of the multiplier block coupled to a first input of the second adder block, the second adder block receiving a second input (c(i))

and an output of the second adder block is coupled to an input of the register block, an output of the register block coupled to a third input of the second adder block.

10. The computational kernel according to claim 9, wherein the two inputs to the first adder block (a(i) and e(i)) and the additional input to the second adder block (c(i)) are input data each respectively associated with a unity coefficient and the additional input to the multiplier block being a coefficient.

11. A system for computation of an IDCT comprising:

(a) a data loader block;

(b) a plurality of MAAC kernels, wherein the plurality of MAAC kernels are coupled to the data loader block.

12. The system according to claim 11, wherein each MAAC kernel includes:

a multiplier block;

an adder block;

a register block;

wherein an output of the multiplier block is coupled to a first input of the adder block, an output of the adder block is coupled to an input of the register block and an output of the register block is coupled to a second input of the adder block, the adder block receiving a third input.

13. The system according to claim 11, wherein the plurality of MAAC kernels are arranged such that any two MAAC kernels share a common multiplier block.

14. A system for performing a computation generally expressible in the form $d = \sum_{i=0}^{N-1} a(i) * b(i)$ comprising:

(a) a plurality of MAAC kernels, wherein each MAAC kernel includes:

a multiplier block;

an adder block;

a register block;

wherein an output of the multiplier block is coupled to a first input of the adder block, an output of the adder block is coupled to an input of the register block and an output

of the register block is coupled to a second input of the adder block, the adder block receiving a third input.

15. The system according to claim 14, wherein the general expression $d = \sum_{i=0}^{N-1} a(i) * b(i)$ may be expressed as $d = c\left(\sum_{i=0}^{M-1} a(i) * b'(i) \right)$ where 'c' is a common factor and at least one of the b'(i)'s is unity.

16. The system according to claim 14, wherein the additional input at each adder block for each of the plurality of MAAC kernels is an input term associated with a coefficient b'(i) being unity.

17. A system for performing downsampling computations:

(a) at least one AMAAC kernel, wherein each AMAAC kernel includes:

a multiplier block;

a first adder block;

a second adder block

a register block;

wherein the first adder block receives two inputs (e(i) and a(i)) and an output of the first adder block is coupled to a first input of the multiplier block, the multiplier block receiving a second input (b(i)) and an output of the multiplier block coupled to a first input of the second adder block, the second adder block receiving a second input (c(i)) and an output of the second adder block is coupled to an input of the register block, an output of the register block coupled to a third input of the second adder block;

(b) at least one MAAC kernel, wherein each MAAC kernel includes:

a multiplier block;

an adder block;

a register block;

wherein an output of the multiplier block is coupled to a first input of the adder block, an output of the adder block is coupled to an input of the register block and an output of the register block is coupled to a second input of the adder block, the adder block receiving a third input.

18. The system according to claim 17, wherein the downsampling computations are performed as part of a video decoding system.